What is claimed is:

1. A low power a reconfigurable processor core, comprising:

one or more processing units, each unit having a clock input that controls the performance of the unit; and

a controller having a plurality of clock outputs each coupled to the clock inputs of the processing units, the controller varying the clock frequency of each processing unit to optimize power consumption and processing power for a task.

2. The processor core of claim 1, wherein one of the processing unit comprises a digital signal processor (DSP).

3. The processor core of claim 1, wherein one of the processing unit comprises a reduced instruction set computer (RISC) processor.

4. The processor core of claim 1, wherein each unit is dynamically managed on a per-task basis.

5. The processor core of claim 1, wherein each unit is clocked at the lowest rate possible to reduce peak power dissipation, reduce average power dissipation, or minimize buffer memory size and power.

6. The processor core of claim 1, wherein the controller generates a plurality of clock signals, each independently rate controlled to each processing unit.

7. The processor core of claim 6, wherein the plurality of clocks is derived from a master clock.

8. The processor core of claim 1, wherein the plurality of clocks comprise gated versions of a master clock.

9. The processor core of claim 1, wherein the controller changes the clock rate of each processing unit independently of the remaining processing unit.

10. The processor core of claim 9, wherein the clock rate is generated based on an algorithm.

11. The processor core of claim 10, wherein the algorithm is optimized for one of the following: power reduction, buffer memory management, or emissions control.

12. The processor core of claim 11, wherein the algorithm is pre-assigned based upon tasks or routines handled by each processing unit.

13. The processor core of claim 11, wherein the algorithm is invoked by one or more external or internal system stimuli.

14. The processor core of claim 1, wherein the controller changes on or more clock inputs on-the-fly.

15. The processor core of claim 1, wherein the controller controls one or more clock inputs in a centralized manner.

16. The processor core of claim 1, wherein the controller controls one or more clock inputs in a decentralized manner.

17. The processor core of claim 1, wherein the controller generates one or more clock inputs in any arbitrary increments from a master clock.

18. The processor core of claim 1, wherein the controller controls one or more clock inputs in a centralized manner.

19. The processor core of claim 1, further comprising a buffer coupled between two processing units.

20. The processor core of claim 19, wherein the buffer is a first-in-first-out (FIFO) buffer.